WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a RAM for use in processing incorporated in a data processing system and to be tested;

a built-in self test circuit for making a built-in self test on said RAM for use in processing; and

a RAM for tester for storing results of said built-in self test on said RAM for use in processing made by said built-in self test circuit so that the results of said built-in self test can be read out by an external tester;

a RAM having a data read-out margin greater than a data read-out margin of said RAM for use in processing being used as said RAM for tester.

2. A semiconductor device comprising:

a plurality of RAMs for use in processing incorporated in a data processing system and to be tested; and

a built-in self test circuit for making a built-in self test on said RAMs for use in processing;

when said built-in self test circuit makes the built-in self test on a part of said plural RAMs for use in processing, a RAM for use in processing, which is not to be tested in said built-in self test,

being used as a RAM for tester which stores results of said built-in self test on said RAM(s) for use in processing made by said built-in self test circuit so that the results of said built-in self test can be read out by an external tester.

3. The semiconductor device according to claim 2, wherein each of said plural RAMs for use in processing comprises a margin widening means for increasing a bit line amplitude at the time of a start of a sense amplifier of said RAM to widen a data read-out margin.

4. The semiconductor device according to claim 3, wherein said margin widening means comprises a delay circuit for gradually delaying a start timing of said sense amplifier according to a signal fed from the outside.

5. The semiconductor device according to claim 3, wherein said margin widening means changes a setting so that a data read-out margin of a RAM used as a RAM for tester among said plural RAMs for use in processing is greater than a data read-out margin of a RAM for use in processing to be tested in said built-in self test.

6. The semiconductor device according to claim 4,

wherein said margin widening means changes a setting so that a data read-out margin of a RAM used as a RAM for tester among said plural RAMs for use in processing is greater than a data read-out margin of a RAM for use in processing to be tested in said built-in self test.

7. The semiconductor device according to claim 3, wherein each of said plural RAMs for use in processing (further) comprises an extending circuit for extending a pre-charge release period.

8. The semiconductor device according to claim 4, wherein each of said plural RAMs for use in processing (further) comprises an extending circuit for extending a pre-charge release period.

9. The semiconductor device according to claim 5, wherein each of said plural RAMs for use in processing (further) comprises an extending circuit for extending a pre-charge release period.

10. The semiconductor device according to claim 6, wherein each of said plural RAMs for use in processing (further) comprises an extending circuit for extending a pre-charge release period.

11. The semiconductor device according to claim 3, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

12. The semiconductor device according to claim 4, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

13. The semiconductor device according to claim 5, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

14. The semiconductor device according to claim 6, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

15. The semiconductor device according to claim 7, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

16. The semiconductor device according to claim 8, wherein each of said plural RAMs for use in processing

further comprises an extending circuit for extending a word selection period.

17. The semiconductor device according to claim 9, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

18. The semiconductor device according to claim 10, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word selection period.

19. A testing apparatus built in a semiconductor device comprising a RAM for use in processing incorporated in a data processing system and to be tested, said testing apparatus comprising:

a built-in self test circuit for making a built-in self test on said RAM for use in processing; and

a RAM for tester for storing results of said built-in self test on said RAM for use in processing made by said built-in self test circuit so that the results of said built-in self test can be read out by an external tester;

a RAM having a data read-out margin greater than a data read-out margin of said RAM for use in

processing being used as said RAM for tester.

20. A testing apparatus built in a semiconductor device comprising a plurality of RAMs for use in processing incorporated in a data processing system and to be tested, said testing apparatus comprising:

a built-in self test circuit for making a built-in self test on said plural RAMs for use in processing;

when said built-in self test circuit makes the built-in self test on a part of said plural RAMs for use in processing, a RAM for use in processing, which is not to be tested in said built-in self test, being used as a RAM for tester which stores results of said built-in self test on said RAM(s) for use in processing made by said built-in self test circuit so that the results of said built-in self test can be read out by an external tester.

21. The testing apparatus for a semiconductor device according to claim 20, wherein each of said plural RAMs for use in processing comprises a margin widening means for increasing a bit line amplitude at the time of a start of a sense amplifier of said RAM to widen a data read-out margin.

22. The testing apparatus for a semiconductor device

according to claim 21, wherein said margin widening means comprises a delay circuit for gradually delaying a start timing of said sense amplifier according to a signal fed from the outside.

23. The testing apparatus for a semiconductor device according to claim 21, wherein said margin widening means changes a setting so that a data read-out margin of a RAM used as a RAM for tester among said plural RAMs for use in processing is greater than a data read-out margin of a RAM for use in processing to be tested in said built-in self test.

24. The testing apparatus for a semiconductor device according to claim 22, wherein said margin widening means changes a setting so that a data read-out margin of a RAM used as a RAM for tester among said plural RAMs for use in processing is greater than a data read-out margin of a RAM for use in processing to be tested in said built-in self test.

25. The testing apparatus for a semiconductor device according to claim 21, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a pre-charge release period.

26. The testing apparatus for a semiconductor device

according to claim 22, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a pre-charge release period.

27. The testing apparatus for a semiconductor device according to claim 23, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a pre-charge release period.

28. The testing apparatus for a semiconductor device according to claim 24, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a pre-charge release period.

29. The testing apparatus for a semiconductor device according to claim 21, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

30. The testing apparatus for a semiconductor device according to claim 22, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

31. The testing apparatus for a semiconductor device according to claim 23, wherein each of said plural RAMs for use in processing further comprises an extending

circuit for extending a word line selection period.

32. The testing apparatus for a semiconductor device according to claim 24, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

33. The testing apparatus for a semiconductor device according to claim 25, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

34. The testing apparatus for a semiconductor device according to claim 26, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

35. The testing apparatus for a semiconductor device according to claim 27, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.

36. The testing apparatus for a semiconductor device according to claim 28, wherein each of said plural RAMs for use in processing further comprises an extending circuit for extending a word line selection period.